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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

*Ex parte* ALEXANDER G. MACINNIS and VIVIAN HSIUN

_____

Appeal 2009-008045
Application 10/786,195
Technology Center 2100

_____

Before JAMES D. THOMAS, JOHN A. JEFFERY, and JAMES R.
HUGHES, *Administrative Patent Judges*.

J. THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134 (a) from the Examiner's final rejection of claims 1 through 27. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

### Invention and Representative Claim

Claim 1 itself is best representative of the disclosed and claimed invention:

1.     A media processing filter engine operable to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:
      a first memory unit to store blocks of media data to be processed;
      a second memory unit operable to store blocks of media data to be processed; and
      a single instruction, multiple data (SIMD) processor operable to receive blocks of media data from the first and second memory units and to simultaneously perform filtering operations on blocks of media data from the first and second memory units.

### Prior Art and Examiner's Rejection

The Examiner relies on the following reference as evidence of anticipation:

| Wu | 5,659,780 | Aug. 19, 1997 |
|---|---|---|

All claims on appeal, claims 1 through 27, stand rejected under 35 U.S.C. §102(b) as being anticipated by Wu.

## ANALYSIS

We affirm the anticipation rejection before us essentially for the reasons set forth by the Examiner in the Answer. We add the following points of emphasis.

Each of the various embodiments in figures 1, 10, 13, 15, 17, 20, 24, 25, 29, and 30 of Wu's pipelined SIMD array processor utilizes a shared memory M characterized as a multiport memory. As illustrated in representative figure 1 of Wu, we agree with the Examiner's characterization that the various output ports illustrated in each of these figures as output ports from the multiport memory M meet the limitation of respective first and second memory units in independent claims 1, 10, and 19. We are unpersuaded by Appellants' arguments in the principal Brief and Reply Brief that this multiport memory M in Wu is a single memory unit, whereas the arguments focus upon the limitations of the claimed first and second memory units constituting separate, apparently, physical memories. We strongly agree with the Examiner's view at the top of page 4 of the answer that "associating an output port with [*sic* - within] M defines one memory unit and associating another output port with [*sic* - within] M defines another memory unit." The Examiner's position is consistent with what a person of ordinary skill in the art would have understood would be a partitioned or multiport memory as taught in Wu. Each port of memory M appears separately addressable.

These views appear to us to be consistent with Appellants' characterization of their own memory elements illustrated in figure 2 of the disclosed invention. Illustrated are separate memory elements 204, 206, and 208. As stated in specification paragraph [29], the associated processor "202

includes a split X-memory comprising memory element X1 204 and X0 206, which allow for simultaneous operations." Thus, the disclosed basis of the claimed disputed elements is in fact a single memory that has been split or otherwise partitioned into separate identifiable portions. Skilled artisans would therefore consider the teachings in Wu to be consistent with the disclosed basis of the claimed and argued features.

The argument relating to the absence of the teaching of media data at page 7 of the principal Brief on appeal has been addressed by the Examiner by identifying certain teachings within column 1 of Wu. In this regard, Wu teaches the environment of use of his invention for video image processors and televisions. Indeed, figures 29 and 30 are characterized as image processing architectures. From these characterizations, a person of ordinary skill in the art would consider the "reusable datum" identified at Wu's column 1, line 48, and the corresponding teaching associated with the figure 1 embodiment at column 4, line 8 as being pixel data. In this regard as well, the claimed blocks of media data are also suggested in the figure 27's illustration of one of Wu's embodiments by identifying data elements as blocks of data. The Reply Brief does not further contest the nature of the data processed within Wu.

Lastly, independent claim 10 recites slightly more specifically that an argued feature relating to shifting the contents of shift registers by a predetermined number of bits corresponding to the size of a data element. This feature is in turn further refined in independent claim 19 by the additional modifier of "a multiple" of the size of the data element. The more focused argument as to these claimed features pertinent to these two independent claims at page 2 of the Reply Brief refers to the disclosed basis

in specification paragraph [49]. The arguments here appear to invite us to read the detailed disclosed teachings of preferred bit widths of pixel data in this noted paragraph into the more broadly defined size characterizations in independent claims 10 and 19 on appeal. This we will not do.

The discussion beginning at column 3 of the shifting functions by means of control signals associated with the figure 1 embodiment in Wu indicates more specifically, beginning at column 4, that the shifting occurs with respect to the entire contents of the shift registers illustrated in this figure, where the contents within any shift register is generically defined in Wu as the earlier-noted "input datum". Therefore, consistent with our earlier discussion with respect to the manner in which a person of ordinary skill in the art would interpret this broad teaching to embodiments utilizing video processing and television techniques, this would amount to the general teaching of pixel information as being a specific form of input data in Wu. Whatever the bit size of an input datum is in Wu, it is shifted a corresponding number of bit positions. The use of the additional modifier "multiple" in independent claim 19 includes, as argued by the Examiner, a multiple of 1.

## DECISION

Since Appellants have not shown that the Examiner erred in the rejection before us under 35 U.S.C. § 102, the rejection of all claims on appeal, claims 1 through 27, on this statutory basis is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(v).

<u>AFFIRMED</u>

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